REMARKS

Status of Claims:

Claims 2-4, 26, and 28 are cancelled. New claims 33-34 are added. Thus, claims 1, 5-25, 27, and 29-34 are present for examination.

Attorney Docket Number:

Applicant points out that in the two previously filed amendments (filed 10/08/04 and 04/29/05), applicant requested that the attorney docket number be amended to be 024299-0352. Applicant notes that the Examiner has not amended the attorney docket number. Thus, applicant again requests that the attorney docket number be amended to be 024299-0352.

Claim Rejection under 35 U.S.C. 112:

Claims 1-10 and 25-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Claims 2-4, 26, and 28 are cancelled. With respect to claims 1, 5-10, 25, 27, and 29-31, as amended, the rejection is respectfully traversed.

The Examiner stated in the Advisory Action:

> "In response to applicant's argument that the recitation of 'modifying' is supported in the original specification. If applicant believes that if address data is incremented then it is modified then Examiner hereby will withdraw the 35 U.S.C. 112, first paragraph rejection".

Applicant does believe that if address data is incremented then it is modified. Thus, claims 1, 5-10, 25, 27, and 29-31 are believed to be in compliance with the requirements of 35 U.S.C. 112, first paragraph. Therefore, applicant requests that the Examiner withdraw the rejection under 35 U.S.C. 112, first paragraph.

Claim Rejection under 35 U.S.C. 102:

Claims 11-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Andreas (Pub. No. US 2004/0093450).

With respect to claims 11-24, as amended, the rejection is respectfully traversed.

Independent claim 11, as amended, recites an electronic device, comprising:

> "a controller;
>
> a plurality of integrated circuits (ICs) addressable by the controller; and
>
> a shared bus joining the controller and the plurality of integrated circuits;
>
> wherein the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first address of the series of addresses,
>
> wherein each IC of the plurality of ICs comprises:
>
> an input for receiving an input enable signal;
>
> an output for providing an output enable signal to another IC in conjunction with a change in address data on the shared bus;
>
> a shared bus input for receiving addresses present on the shared bus; and
>
> means for storing an address present on the shared bus as an address of the IC in response to receiving the input enable signal;
>
> wherein the input of a first IC of the plurality of ICs communicates with the output of the controller, and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration;
>
> wherein the first address of the series of addresses produced by the controller on the shared bus represents an address of the first IC on the shared bus, and each succeeding address of the series of addresses produced by the controller on the shared bus represents an address of a corresponding succeeding IC in the daisy chain configuration; and

wherein the enable signal produced on the output of the controller is received at the input of the first IC as the input enable signal for the first IC, and the output enable signal provided on the output of each IC of the plurality of ICs is received at the input of a corresponding succeeding IC in the daisy chain configuration as the input enable signal for the corresponding succeeding IC." (Emphasis Added).

An electronic device including the above-quoted features has at least the advantages that: (i) a controller is joined to a plurality of ICs by a shared bus; (ii) the controller is programmed to produce a series of addresses on the shared bus and to produce an enable signal on an output in conjunction with a first addresses of the series of addresses; (iii) each IC has an input for receiving an input enable signal, an output for providing an output enable signal to another IC in conjunction with a change in address data on the shared bus, a shared bus input for receiving addresses present on the shared bus, and a means for storing an address present on the shared bus as an address of the IC in response to receiving the input enable signal; (iv) the input of a first IC communicates with the controller, and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a daisy chain configuration; (v) the first address of the series of addresses represents an address of the first IC on the shared bus, and each succeeding address of the series of addresses represents an address of a corresponding succeeding IC; and (vi) the enable signal produced on the output of the controller is received at the input of the first IC, and the output enable signal provided on the output of each IC is received at the input of a corresponding succeeding IC in the daisy chain configuration as the input enable signal for the corresponding succeeding IC. (FIGs. 2, 5, and 6; Specification; page 2, line 26 to page 3, line 4; page 6, line 7 to page 8, line 7).

Andreas neither discloses nor suggests an electronic device including the above-quoted features. In a first embodiment of Andreas that is illustrated in FIG. 1 of Andreas, the serial device slaves 120-150 do not have an output for providing an output enable signal to another serial device slave in conjunction with a change in address data on the common serial communication bus 160. (Andreas; FIG. 1). Instead, in the first embodiment of Andreas, the serial bus master 110 must be capable of providing individual chip selects (one for each serial

device slave), where the chip select input for each serial device slave 120-150 is asserted by the serial bus master 110 to indicate that the chip should respond to information being broadcast on the serial communication bus 160. (Andreas; FIG. 1; paragraph [0024]).

Thus, in the first embodiment of Andreas, the serial bus master 110 must have a separate chip select line 172-178 for each serial device slave 120-150, which imposes a requirement that the serial bus master 110 have dedicated pins to handle the individual chip select signals 172-178. (Andreas; FIG. 1; paragraph [0024]). Indeed, Andreas even recognizes that, "[o]ne disadvantage of this technique is the imposed requirement for dedicated pins or exclusive signal lines on the processor to handle the device select signals." (Andreas; paragraph [0004]) (Emphasis Added). Also, applicant has noted that pins are scarce in miniaturized circuits, and one of the problems that embodiments of the present invention seek to address is that conventional systems require too many dedicated pins on a controller in order to assign addresses to ICs. (Applicant's FIG. 1; Specification; page 1, line 26 to page 2, line 6; page 2, lines 15-19).

In contrast, an electronic device including the above-quoted features allows for an output of a controller to communicate with an input of a first IC and for inputs of succeeding ICs to communicate with outputs of preceding ICs in a daisy chain configuration, where an enable signal produced on the output of the controller is received at the input of the first IC as an input enable signal for the first IC, and an output enable signal provided on the output of each IC is received at the input of a corresponding succeeding IC in the daisy chain configuration as an input enable signal for the corresponding succeeding IC. Thus, an electronic device including the above-quoted features allows for reducing a number of dedicated pins required on a controller for assigning addresses to ICs as compared with conventional systems. (Applicant's FIG. 2).

In a second embodiment of Andreas as illustrated in FIG. 2 of Andreas, the serial device slaves 220-250 also do not have an output for providing an output enable signal to another serial device slave in conjunction with a change in address data on the shared communication bus 260. (Andreas; FIG. 2). Indeed, in the second embodiment of Andreas, the serial bus master 210 cannot even produce addresses on the shared communication bus 260, because the shared

communication bus 260 only includes a clock signal SCLK 262 from the serial bus master 210 to the serial device slaves 220-250, and a serial data out SDO 266 from the serial device slaves 220-250 to the serial data in of the serial bus master 210. (Andreas; FIG. 2; paragraph [0026]-[0028]). Instead, in the second embodiment of Andreas, a mask value must be serially clocked through each serial device slave 220-250 before each command to specify which serial device slaves are enabled and which are disabled for the command. (Andreas; paragraphs [0036] and [0040]). The mask value in the second embodiment of Andreas is not produced on the shared communication bus 260, but is provided by the SDI_THRU from each serial device slave to a succeeding serial device slave. (Andreas; FIG. 2, references 224, 234, 244, 254; paragraph [0036]). Indeed, Andreas specifically states that, "[t]he SDI signal is not part of the shared communication bus 260." (Andreas; paragraph [0026]) (Emphasis Added).

In contrast, an electronic device including the above-quoted features allows for a controller to be programmed to produce a series of addresses on a shared bus, and for each IC to have an input for receiving an input enable signal, an output for providing an output enable signal to another IC in conjunction with a change in address data on the shared bus, a shared bus input for receiving addresses present on the shared bus, and means for storing an address present on the shared bus as an address of the IC in response to receiving the input enable signal.

Therefore, independent claim 11, as amended, is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable. Because they depend from independent claim 11, dependent claims 12-19, 32, and 34 are believed to be allowable for at least the same reasons that independent claim 11 is believed to be allowable.

Independent claim 20, as amended, recites an electronic device, comprising:

> "means for generating an enable signal at an output of a controller and generating first address data on a shared bus;
>
> means for receiving the enable signal generated at the output of the controller at an input of a first integrated circuit (IC);

means for receiving the first address data at a shared bus input of the first IC;

means for storing the first address data in an address register of the first IC as an address of the first IC upon coincidence of receiving the enable signal and receiving the first address data; and

means for providing an output enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus." (Emphasis Added).

An electronic device including the above-quoted features has at least the advantages that: (i) means for generating generates an enable signal at an output of a controller and generates first address data on a shared bus; (ii) means for storing stores the first address data in an address register of the first IC as an address of the first IC upon coincidence of receiving the enable signal and receiving the first address data; and (iii) means for providing provides an output enable signal at an output of the first IC to an input of a second IC in conjunction with a change in address data on the shared bus.

Independent claim 20 is believed to be allowable for at least the same reasons indicated above with respect to claim 11 where it was pointed out that the serial device slaves in the embodiments of Andreas do not have an output for providing an output enable signal to another serial device slave in conjunction with a change in address data on a shared communication bus.

Therefore, independent claim 20 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable.

Independent claim 21 recites a method with features similar to features of an electronic device of independent claim 20 and, thus, independent claim 21 is believed to be allowable for at least the same reasons that independent claim 20 is believed to be allowable. Because they depend from independent claim 21, dependent claims 22-24 are believed to be allowable for at least the same reasons that independent claim 21 is believed to be allowable.

Claim Rejection under 35 U.S.C. 103:

Claims 1-10 and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andreas (Pub. No. US 2004/0093450) in view of Floyd et al. (U.S. Patent Number 6,529,979) (hereinafter Floyd).

Claims 2-4, 26, and 28 are cancelled. With respect to claims 1, 5-10, 25, 27, and 29-31, as amended, the rejection is respectfully traversed.

Independent claim 1, as amended, recites an electronic device, comprising:

> "a controller programmed to produce first address data on an output thereof;
>
> a plurality of integrated circuits (ICs) addressable by the controller; and
>
> a shared bus, said <u>shared bus</u> joining the controller and the plurality of ICs <u>such that the controller is able to send data to the plurality of ICs over the shared bus</u>;
>
> wherein each IC of the plurality of ICs comprises:
>
> an input for receiving address data, said address data <u>representing an address of the IC on the shared bus</u>;
>
> an address register for storing the received address data <u>as the address of the IC on the shared bus</u>;
>
> output generator logic for <u>modifying</u> the <u>received address data</u> to produce <u>modified address data</u> that is <u>different from</u> the received address data, said modified address data <u>representing an address of another IC on the shared bus</u>; and
>
> an output for providing the <u>modified</u> address data;
>
> wherein the input of a first IC of the plurality of ICs communicates with the output of the controller, and the inputs of succeeding ICs communicate with the outputs of preceding ICs in a <u>daisy chain configuration</u>;
>
> wherein the <u>first address data</u> produced on the output of the controller <u>represents an address of the first IC</u> on the shared bus; and

> wherein the modified address data provided on the output of each IC of the plurality of ICs represents an address of a corresponding succeeding IC in the daisy chain configuration on the shared bus." (Emphasis Added).

An electronic device including the above-quoted features has at least the advantages that: (i) a controller is joined to a plurality of ICs by a shared bus such that the controller is able to send data to the plurality of ICs over the shared bus; (ii) each IC has an input for receiving address data, where the address data represents an address of the IC on the shared bus, and output generator logic for modifying the received address data to produce modified address data that is different from the received address data, where the modified address data represents an address of another IC on the shared bus; (iii) the input of a first IC of the plurality of ICs communicates with an output of the controller, and the inputs of succeeding ICs communicate with outputs of preceding ICs in a daisy chain configuration; and (iv) the modified address data provided on the output of each IC of the plurality of ICs represents an address of a corresponding succeeding IC in the daisy chain configuration on the shared bus. (FIGs. 2, 3, and 4; Specification; page 2, lines 20-26; page 4, line 23 to page 5, line 11).

Neither Andreas nor Floyd, alone or in combination, disclose or suggest an electronic device including the above-quoted features. The Examiner recognizes that Andreas does not disclose an IC providing modified address data different from received address data. The Examiner then points to Floyd as disclosing an address packet modified in a variety of different manners to provide an indication of a positive acknowledgement, and states that, "[i]t would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Floyd's teaching into Andreas's system so as to have the advantages to improve communication system and protocol for dedicated configuration to minimizes the amount of circuitry and wire congestion." (Emphasis Added).

However, Floyd does not disclose or suggest that an IC modifies received address data to produce modified address data that is different from the received address data, where the modified address data represents an address of another IC on a shared bus. As shown in FIG. 4B of Floyd, in the system of Floyd, an address packet consists of 19 bits, consisting of a start bit, a

read/write bit, 16 address bits, and a stop bit. (Floyd; FIG. 4B; column 6, lines 41-45). In order to provide a positive acknowledgement of a receipt of an address packet back to a central source, a satellite in the system of Floyd modifies the address packet by clearing the stop bit of the address packet or otherwise modifying the packet to indicate acceptance of the packet. (Floyd; abstract). Floyd teaches away from modifying the address packet to modify the 16 address bits in the address packet to represent an address of another satellite, because Floyd only wants the converter 500 of the satellite specified by the 16 address bits in the address packet from the central source to match the 16 address bits. Indeed, Floyd states that, "[s]ince all converters have a unique address, it is the only converter that will match; all of the other converters, after they receive the address packet, will not match on that particular address packet." (Floyd; column 7, lines 51-54) (Emphasis Added).

Furthermore, even if the system of Floyd were combined with the system of Andreas to allow the serial device slaves in the system of Andreas to receive address data and provide modified address data, where the modified address data represents an address of another serial device slave on the shared communication bus, the resulting system would not operate properly. The embodiment of Andreas with a daisy chain configuration is illustrated in FIG. 2 of Andreas. In the embodiment of FIG. 2 of Andreas, a mask value is distributed by the serial bus master 210, where the serial bus master 210 sets each bit of the mask value to specify whether a serial device slave corresponding to the bit should be enabled or disabled for an operation. Suppose that the serial bus master 210 of the system of Andreas only wants the first serial device slave 220 to be enabled for an operation. If the first serial device slave 220 modifies the mask value to change the bit in the mask value corresponding to the serial device slave 230, then the serial device slave 230 would be enabled for an operation when the serial bus master 210 actually wanted the serial device slave 230 to be disabled for the operation. (Andreas; FIG. 2). Thus, allowing for each of the serial device slaves 220-250 in the system of Andreas to modify the mask value to provide a modified mask value to enable another serial device slave would cause the resulting system to not function properly. Indeed, Andreas teaches away from modifying the mask value, because Andreas specifically states that, "the SDI THRU signal for a device should be the same as the

clocked SDI signal for that device while the mask value is being distributed." (Andreas; paragraph [0036]) (Emphasis Added).

Moreover, the mask value in the system of Andreas is never returned to the serial bus master 210 after being clocked through the serial device slaves 220-250, so there would also be no motivation to modify the mask value to provide a positive acknowledgement back to the serial bus master 210. (Andreas; FIGs. 2-3). Also, as applicant stated in the reply filed on October 8, 2004, the mask value in the system of Andreas is not an address of an IC on a shared bus, and each serial device slave 220-250 in the system of Andreas only checks a corresponding bit of the mask value to determine whether it is enabled or disabled for a particular operation. (Andreas; paragraphs [0040] – [0041]).

Therefore, independent claim 1, as amended, is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable. Because they depend from independent claim 1, dependent claims 5-7, 25, 27, and 33 are believed to be allowable for at least the same reasons that independent claim 1 is believed to be allowable.

Independent claim 8, as amended, recites an electronic device, comprising:

> "means for generating first address data at an output of a controller;
>
> means for receiving the first address data at an input of a first integrated circuit (IC);
>
> means for storing the first address data in the first IC as an address of the first IC;
>
> means for modifying the first address data in the first IC to produce first modified address data different from the first address data; and
>
> means for providing the first modified address data to a second IC through an output of the first IC, said first modified address data representing an address of the second IC." (Emphasis Added).

An electronic device including the above-quoted features has at least the advantages that: (i) means for generating generates first address data at an output of a controller; (ii) means for

storing stores the first address data in a first IC as an address of the first IC; (iii) means for modifying modifies the first address data in the first IC to produce first modified address data different from the first address data; and (iv) means for providing provides the first modified address data to a second IC through an output of the first IC, where the first modified address data represents an address of the second IC.

Independent claim 8 is believed to be allowable for at least the same reasons indicated above with respect to independent claim 1, where it was pointed out that Floyd does not disclose or suggest that an IC modifies received address data to produce modified address data that is different from the received address data, where the modified address data represents an address of another IC on a shared bus, and that even if the system of Floyd were combined with the system of Andreas to allow the serial device slaves in the system of Andreas to receive address data and provide modified address data representing an address of another serial device slave on the shared communication bus, the resulting system would not operate properly.

Therefore, independent claim 8 is neither disclosed nor suggested by the cited prior art and, hence, is believed to be allowable. Because it depends from independent claim 8, dependent claim 29 is believed to be allowable for at least the same reasons that independent claim 8 is believed to be allowable.

Independent claim 9 recites a method with features similar to features of an electronic device of independent claim 8. Therefore, independent claim 9 is believed to be allowable for at least the same reasons that independent claim 8 is believed to be allowable. Because they depend from independent claim 9, dependent claims 10, 30, and 31 are believed to be allowable for at least the same reasons that independent claim 9 is believed to be allowable.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 50-0872. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 50-0872.

If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 50-0872.

Respectfully submitted,

Date July 11, 2005

By [signature]

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